

Generalized Parameter Extraction Method for Analog Circuit Fault Diagnosis

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Abstract—The symbolic technique for analog fault diagnosis is presented in this paper. The cancellation-free Generalized Parameter Extraction Method for parametric fault diagnosis of electronic circuits is considered. The topological conditions of diagnosability of the active analog circuit are discussed. The algorithm for automotive fault diagnosis is proposed and implemented with the Cirsym symbolic analyzer. The experimental results on a filter circuit show the efficiency and reliability of proposed technique.

Keywords—*fault diagnosis; electronic circuits; nullor; symbolic techniques; testability analysis*

I. INTRODUCTION

The fault detection and diagnosis of analog circuits is an important research area where a number of corresponding theories and techniques have been developed [1–13]. Fault diagnosis approaches are usually classified into two main categories: simulation-before-test, including probabilistic and fault dictionary techniques, and simulation-after-test, including optimization, fault verification, and parameter identification techniques.

The fault dictionary method compared the fault values of the unknown conditions of the circuit under test with those stored in the dictionary to match one of the predefined faults according to preset criteria [1]. This is one of the most used methods. The neural network [6, 7] is a popular technique to build up a fault dictionary. Despite the advantages of fault dictionary, there are still persistent challenges, such as test point selection and potential faults simulations. To obtain the differences between the faulty circuit response and fault-free circuit response, wavelet technology can be used [7].

In parametric fault diagnosis procedures, the unknown quantities are the actual component values. The measurements are performed in the frequency domain. The number of measurements must be not less than amount of unknown parameters. The problem of diagnosis at a single test frequency for the first time was studied in [8]. This approach was to determine the currents and voltages of desired elements from the measured currents and voltages of certain other elements. But this method requires complicated and inconvenient algorithm for construction of system of equation.

More effective approach to diagnosis at a single test frequency using nullors was proposed in [9]. Nullator-norator models were used instead of the elements with unknown parameters.

Symbolic analysis methods for multi-frequency parametric fault diagnosis were successfully used in [10–12]. Symbolic analysis is a technique for presenting the characteristics of a circuit as closed-form functions, depending on circuit parameters and complex frequency. But the circuit diagnosis at the set of frequencies often deals with system of nonlinear equations and needs special working mode to provide the necessary accuracy and validity [10].

In this paper the symbolic technique based on Generalized Parameter Extraction Method (GPEM) [13–15] for parametric fault diagnosis at a single test frequency is proposed. The description of proposed technique and algorithm for automatic fault diagnosis procedures are presented in Section III and IV correspondingly. The illustrative example can be found in Section IV. Conclusions are summarizing the results of paper.

II. EXPLOITING SYMBOLIC ANALYSIS FOR PARAMITRIC FAULT DIAGNOSIS

The representation of unknown parameters in form of symbolic expressions provides the analysis of the general properties of functions as well as it's solvability. The fault diagnosis can be reduced to symbolic analysis procedure by means of compensation of the elements with unknown parameters by oriented nullor models. The impedances, admittances, controlled sources (CS) and signal sources with unknown parameters are replaced (compensated) by oriented norators [13]. The measuring voltages and currents are modeled by means of oriented nullators and input sources. The circuit transformed in that way is called compensated circuit. The nonzero determinant of compensated circuit is a sufficient condition of diagnosability [8].

GPEM is used for symbolic analysis of compensated circuits in this paper. The main advantage of the method is that it is cancellation-free comparing to matrix-based techniques. An extension of the GPEM for the case of multiple excitations the new circuit element is introduced – nullator controlled multidimensional source [15]. Multidimensional source can consist of an arbitrary number of current and/or

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voltage sources. The controlling nullator is the same for each of them.

In accordance with GPEM the circuit response is a ratio of two circuit determinants [14]. For example, the arbitrary voltage function in complex form can be expressed as

$$\underline{V} = \Delta_N / \Delta_D, \quad (1)$$

where Δ_D is the determinant of the circuit, in which the input excitations are equals to zero, Δ_N is the determinant of the circuit with multidimensional source, in which the signal sources is controlled by nullator inserted instead of voltage \underline{V} . Note that the multidimensional sources are oriented in opposite to input sources.

For example let's consider the test circuit in Fig. 1 (a). The circuit with multidimensional source for calculation of numerator determinant of current I is presented in Fig. 1 (b).

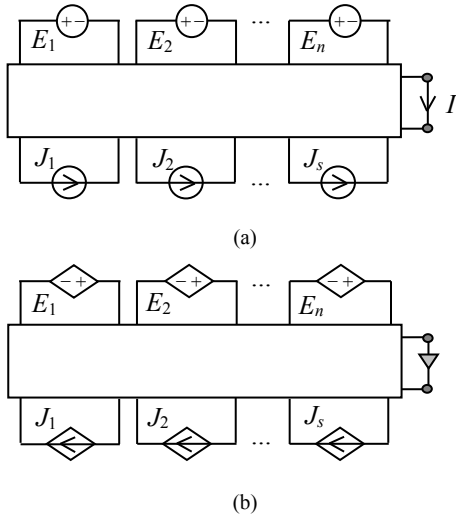


Fig. 1. (a) Test circuit with n input voltage sources and s input current sources. (b) Circuit with nullator controlled multidimensional source.

The calculation procedure of the determinants is based on the recursive usage of the parameter extraction formula [14]:

$$\Delta = \chi \Delta(\chi \rightarrow \infty) + \Delta(\chi = 0), \quad (2)$$

where χ is a parameter of arbitrary linear circuit element, $\Delta(\chi \rightarrow \infty)$ and $\Delta(\chi = 0)$ are corresponding determinants of the circuit matrix in which the parameter of extracted elements $\chi \rightarrow \infty$ or $\chi = 0$ respectively.

Usage (2) to extract parameter E_n in numerator circuit in Fig. 1 (a) we obtained the circuit-algebraic expression shown below:

$$N = E_n \left[\text{Circuit with nullator} \right] + \left[\text{Circuit with nullator} \right] \quad (3)$$

Equation (3) shows the circuit-algebraic expression for the numerator determinant N . It consists of two circuit diagrams in brackets, separated by a plus sign. The first diagram shows a circuit with a nullator (diamond with a '+' sign on the left and a '-' sign on the right) connected in series with a voltage source E_n . The second diagram shows a circuit with a nullator (diamond with a '+' sign on the left and a '-' sign on the right) connected in parallel with a current source J_s . The current source J_s is represented by a diamond with an arrow pointing to the right.

The algorithm for automatic fault diagnosis is presented in Section III.

III. THE ALGORITHM FOR AUTOMATIC FAULT DIAGNOSIS

A. Choosing the circuit nodes for measurements

The amount of measured currents and voltages must be equal to number of unknown parameters. Note that the measured variables must be control-free. The topological conditions for identification of controlled currents and voltages are presented in Table I. These conditions are results from solvability rules for the linear active networks [8]. The measured currents and voltages are represented in Table I by ammeters and voltmeters correspondingly.

Let's consider the topological conditions shown in Table I.

1. All voltmeters must be included into one arbitrary circuit tree. They cannot be connected into loops with voltmeters, with voltage sources, with controlling currents of CS or with nullators (see row 1 in Table I).
2. All ammeters must be included into arbitrary set of circuit links. They cannot formed the circuit cuts with ammeters, with current sources, with controlling voltages of CS or with nullators (see row 2 in Table I).
3. The circuit element with unknown value (two-terminal, input source or controlling source) cannot be connected into loop with elements of the same type, with input voltage sources, with controlled voltage sources or norators (see row 3 in Table I).
4. The circuit element with unknown values cannot form the circuit cuts with elements of the same type, with input current sources, with controlled current sources or with norators (see row 4 in Table I).

The rules presented in first four rows in Table I are necessary but insufficient conditions for diagnosability of circuit. The other causes of circuit degeneracies are possible and some of them are shown in the fifth row in Table I.

B. Formation of compensated circuit

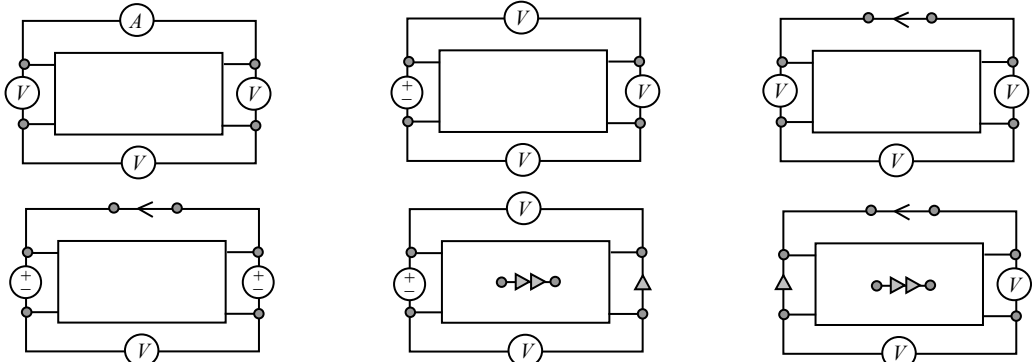
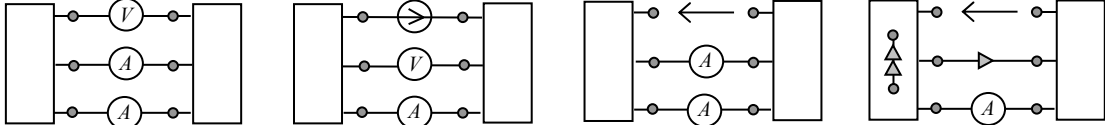
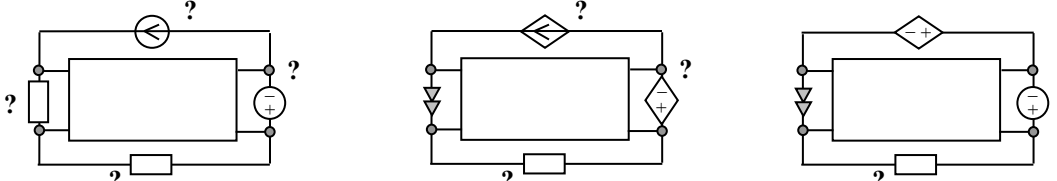
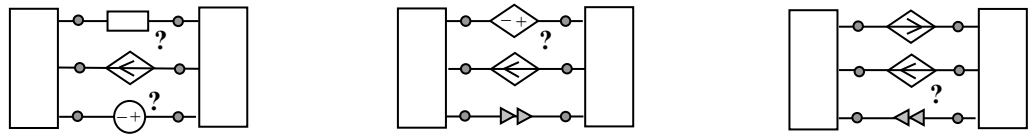
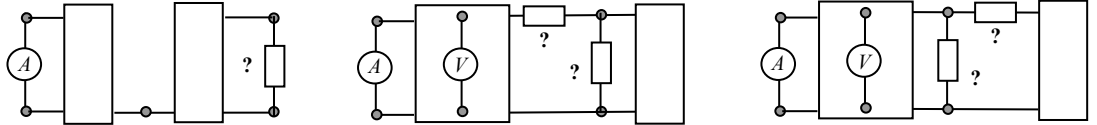
All elements with unknown values (impedances, admittances, input sources, CS) are replaced by norators in compensated circuit. Each voltmeter is replaced by serial connection of input voltage source and nullator, and each ammeter is replaced by parallel connection of input current source and nullator.

The transformation example of circuit with unknown parameters of impedance Z and current controlled current source β_2 is presented in Fig. 2. The equivalence of circuit models shown in Fig. 2 (a) and Fig. 2 (b) is proved in accordance with indirect compensation theorem [13].

Indirect compensation theorem. The impedance element Z in arbitrary linear network presented in Fig. 3 (a) with nonzero circuit determinant can be modeled by means of nullor elements and input voltage source connected between any pair of nodes as it shown in Fig. 3 (b).

As can be seen from circuit shown in Fig. 3 (b) the current at the modeling voltage source E is zero because the source connected in series with nullator. So the source parameter E is equal to measured voltage V in circuit shown in Fig. 3 (a).

TABLE I. CONTROLLING CRITERIONS OF MEASURED VARIABLES

№	Circuit classes
1	<p>Circuits with loop consists of voltmeters, ammeters, voltage sources, controlling currents of CS and nullators</p> 
2	<p>Circuits with cuts consists of voltmeters, ammeters, current sources, controlling voltages of CS and nullators</p> 
3	<p>Circuit with loop consists of elements with unknown parameters, voltage source, controlled voltage sources and norators</p> 
4	<p>Circuit with cuts consists of elements with unknown parameters, current source, controlled current sources and norators</p> 
5	<p>Additional circuits</p> 

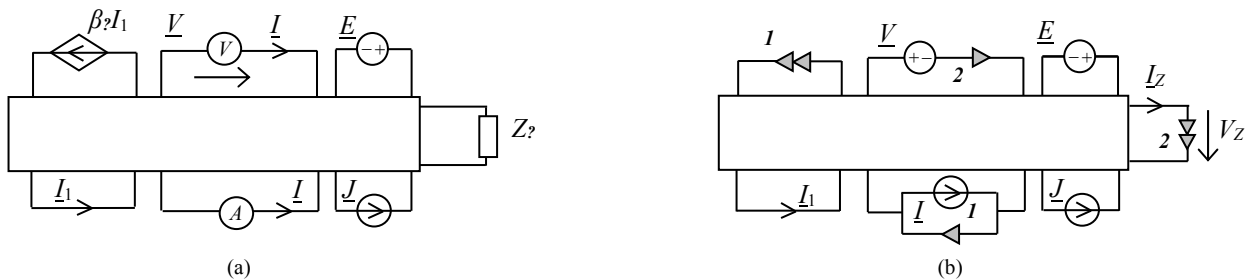


Fig. 2. Transformation example: (a) circuit with unknown parameters; (b) circuit with compensated elements.

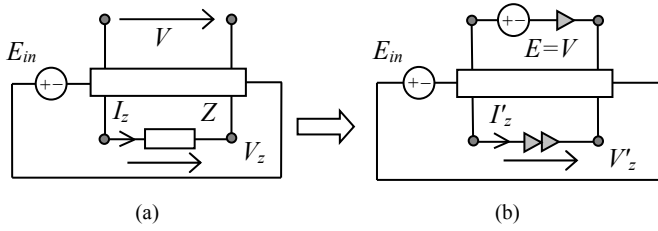


Fig. 3. The example of resistance compensation

The correctness of replacement of impedance Z by norator is confirmed by following identity:

$$V'_z / I'_z = V_z / I_z. \quad (4)$$

In accordance with superposition principle the voltage V'_z and current I'_z can be expressed as:

$$V'_z = K_1 E_{in} + K_2 E \quad \text{and} \quad I'_z = Y_1 E_{in} + Y_2 E, \quad (5)$$

where K_1 and K_2 are the transfer voltage functions, Y_1 and Y_2 are the transfer admittance functions to impedance Z from the sources E_{in} and E correspondingly.

Lets express the voltage/current ratio V'_z / I'_z from (4) in circuit-algebraic form using (5). In accordance with GPEM the calculation of transfer function numerator deals with replacing of input sources by norators and output signals by nullators. Note, that the serial connection of norator and nullator leads to open circuit, while the parallel connection of norator and nullator leads to short:

$$\frac{V'_z}{I'_z} = \frac{\left| \begin{array}{c} \text{Circuit with } E_{in} \text{ as norator and } E \text{ as nullator} \\ \text{Circuit with } E_{in} \text{ as norator and } E \text{ as nullator} \end{array} \right|}{\left| \begin{array}{c} \text{Circuit with } E_{in} \text{ as norator and } E \text{ as nullator} \\ \text{Circuit with } E_{in} \text{ as norator and } E \text{ as nullator} \end{array} \right|}. \quad (6)$$

Now we have to present as circuit-algebraic expression the voltage/current ratio V_z / I_z from (4):

$$\frac{V_z}{I_z} = \frac{\left| \begin{array}{c} \text{Circuit with } I \text{ as norator and } I \text{ as nullator} \\ \text{Circuit with } I \text{ as norator and } I \text{ as nullator} \end{array} \right|}{\left| \begin{array}{c} \text{Circuit with } I \text{ as norator and } I \text{ as nullator} \\ \text{Circuit with } I \text{ as norator and } I \text{ as nullator} \end{array} \right|}. \quad (7)$$

The extraction of parameter Z in expression (7) by means of (2) provide the following identity:

$$E_{in} \left[\left| \begin{array}{c} \text{Circuit with } Z \text{ as norator and } Z \text{ as nullator} \\ \text{Circuit with } Z \text{ as norator and } Z \text{ as nullator} \end{array} \right| + \left| \begin{array}{c} \text{Circuit with } Z \text{ as norator and } Z \text{ as nullator} \\ \text{Circuit with } Z \text{ as norator and } Z \text{ as nullator} \end{array} \right| \right] = \\ = V_{in} \left[\left| \begin{array}{c} \text{Circuit with } Z \text{ as norator and } Z \text{ as nullator} \\ \text{Circuit with } Z \text{ as norator and } Z \text{ as nullator} \end{array} \right| + \left| \begin{array}{c} \text{Circuit with } Z \text{ as norator and } Z \text{ as nullator} \\ \text{Circuit with } Z \text{ as norator and } Z \text{ as nullator} \end{array} \right| \right]. \quad (8)$$

The voltage/current ratio V_z / I_z in circuit shown in Fig. 3 (a) is equal to impedance Z and can be expressed by means of (8) as:

$$\frac{V_z}{I_z} = \frac{\left| \begin{array}{c} \text{Circuit with } -E_{in} \text{ as norator and } +U \text{ as nullator} \\ \text{Circuit with } -E_{in} \text{ as norator and } +U \text{ as nullator} \end{array} \right|}{\left| \begin{array}{c} \text{Circuit with } E_{in} \text{ as norator and } -U \text{ as nullator} \\ \text{Circuit with } E_{in} \text{ as norator and } -U \text{ as nullator} \end{array} \right|}. \quad (9)$$

The expressions (6) and (9) are identical because $V = E$ and inverting the sign of E_{in} in (9) leads to nullator direction changing to opposite [14].

For another circuit element type the indirect compensation theorem can be proved in the same way.

C. Testing of solvability of compensated circuit

Parameters of input sources in compensated circuit are removed, and circuit determinant is calculating by means of GPEM. If the expression of determinant is equal to zero than fault diagnosis does not has solution for chosen voltages and (or) currents measurements. In that case some different nodes must be chosen and algorithm must be restarted.

D. Generation of circuit-algebraic formulae for unknown parameters

Impedances and admittances of the unknown parameters can be calculated as following:

$$Z = -\frac{\Delta_Z}{\Delta^Z}, \quad (10) \quad Y = -\frac{\Delta^Y}{\Delta_Y}, \quad (11)$$

where $\Delta_Z, \Delta^Z, \Delta_Y, \Delta^Y$ – determinants of subcircuits derived from transformed circuit. The upper indexes mean that norator modeling unknown parameter is replaced by short, the bottom indexes mean that norator is deleted.

For example let's express in accordance with (10) the circuit-algebraic formula for arbitrary impedance Z :

$$Z = \frac{V_z}{I_z} = \frac{\left| \begin{array}{c} \text{Circuit with } I \text{ as norator and } I \text{ as nullator} \\ \text{Circuit with } I \text{ as norator and } I \text{ as nullator} \end{array} \right|}{\left| \begin{array}{c} \text{Circuit with } I \text{ as norator and } I \text{ as nullator} \\ \text{Circuit with } I \text{ as norator and } I \text{ as nullator} \end{array} \right|}. \quad (12)$$

For unknown controlled source parameters the circuit-algebraic formulae can be expressed in generalized form:

$$\chi = -\frac{\Delta(\chi=0)}{\Delta(\chi \rightarrow \text{nullor})}, \quad (13)$$

where χ is parameter of any controlled source; $\Delta(\chi=0)$ is determinant of subcircuit in which controlled source parameter χ is zero, and $\Delta(\chi \rightarrow nullor)$ is determinant of subcircuit in which controlled source χ is replaced by nullor.

Circuit-algebraic formulae for unknown quantities of input sources can be expressed as following:

$$\underline{E}_s = \frac{\Delta_{\underline{E}_s}}{\Delta(\underline{E}=0; \underline{J}=0)}, \quad \text{and} \quad \underline{J}_s = \frac{\Delta_{\underline{J}_s}}{\Delta(\underline{E}=0; \underline{J}=0)}, \quad (14)$$

where $\Delta_{\underline{E}_s}$ and $\Delta_{\underline{J}_s}$ are determinants of subcircuits in which the voltage source is shorted and the current source is deleted; $\Delta(\underline{E}=0; \underline{J}=0)$ is determinant of subcircuit in which input sources values are nulling.

E. Generation of symbolic functions for unknown parameters

Symbolic expression for unknown parameter can be calculated from expressions like (10), (11), (13) and (14) using circuit-algebraic formulae (2)–(3) in accordance with GPEM approach.

Presented parametric fault diagnosis algorithm has been implemented by V. Filartov in freeware symbolic circuit analyzer Cirsym (intersyn.net).

IV. EXAMPLE

Let's consider analysis of the circuit of second order low-frequency filter with ideal operational amplifier shown in Fig. 4 (a). The equivalent nullor circuit of filter is presented in Fig. 4 (b). We assume that values of resistances R_1, R_2, R_3, R_4 and R_5 are all known and the symbolic expressions for parameters of capacitors C_1, C_2 and resistance R_6 need to be found. In accordance with proposed algorithm we performed all five steps to obtain the solution.

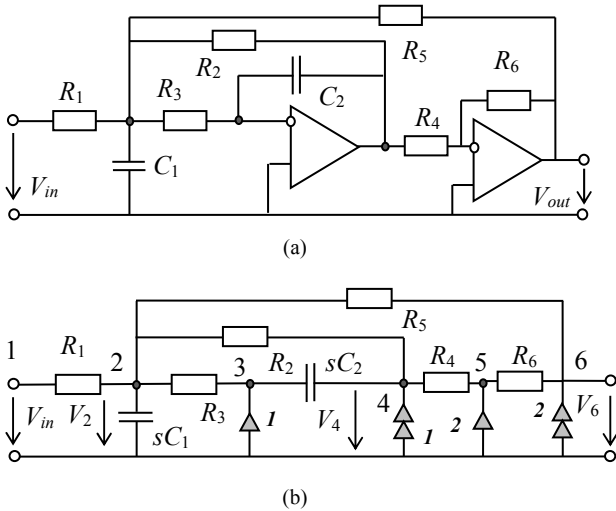


Fig. 4. (a) Second order filter circuit; (b) Equivalent nullor circuit.

A. Lets choose the nodes 2, 4 and 6 for measuring of voltages $\underline{V}_2, \underline{V}_4$ and \underline{V}_6 correspondingly. According to Table I these voltage are control-free.

B. Elements with unknown values C_1, C_2 and resistance R_6 are replaced by norators in compensation circuit, as shown in Fig 5 (a). The measured voltages $\underline{V}_2, \underline{V}_4$ and \underline{V}_6 are replaced by serial connection of voltage sources and nullators. The nullor elements must be numbered sequentially in order of increase.

C. Determinant of transformed circuit with nulling input sources, as shown in Fig. 5 (b), need to be calculated for verification of diagnosability of selected measuring nodes. Each of resistances R_1, R_2, R_3, R_4 и R_5 is forming the loop with norator or nullator so they parameters can be extracted in accordance with GPEM. In that case resistance elements are deleted from the circuit and the determinant of residual circuit will be equal to unity. The symbolic expression of input compensated circuit determinant will be as follow:

$$D = R_1 R_2 R_3 R_4 R_5. \quad (15)$$

So the determinant of compensated circuit is not equal to zero and solution for filter fault diagnosis is exists.

D. The formulae for unknown parameters in accordance with (4) can be expressed as:

$$C_1 = -\frac{\Delta^{sC1}}{p \cdot \Delta_{sC1}}; \quad C_2 = -\frac{\Delta^{sC2}}{p \cdot \Delta_{sC2}}; \quad R_6 = -\frac{\Delta_{R6}}{\Delta^{R6}}, \quad (16)$$

where $\Delta^{sC1}, \Delta^{sC2}, \Delta^{R6}$ and $\Delta_{sC1}, \Delta_{sC2}, \Delta_{R6}$ are determinants of subcircuit derived from compensated circuit in Fig. 5 (a) by shorting of the norators 3, 4, and 5.

For example the circuit-algebraic expression for resistance R_6 will be as following:

$$R_6 = - \frac{\begin{array}{c} \text{Circuit diagram for } R_6 \text{ calculation} \\ \text{Top part: Original circuit with nullors and voltage sources } V_1, V_2, V_4, V_6. \\ \text{Bottom part: Modified circuit with nullors and voltage sources } V_1, V_2, V_4, V_6. \end{array}}{\dots} \quad (17)$$

Note, that input sources are replaced by multidimensional source controlled by nullator with number 5 in expression (17).

E. Next step is expansion of numerator circuit in expression (17) by means of GPEM. The elements of nullor marked by number 2 are connected in parallel and can be shorted. Than the controlled sources with parameter \underline{V}_6 must be extracted and replaced by norator marked by number 5. In that case parameters of all other controlled sources will be null. Each of resistances R_1, R_2, R_3, R_4 и R_5 is forming the loop with norator or nullator so their parameters can be extracted in accordance with GPEM. The determinant of residual circuit is

equal to unity. So the symbolic expression of numerator will be as follow:

$$N = R_1 R_2 R_3 R_4 R_5 \underline{V}_6. \quad (18)$$

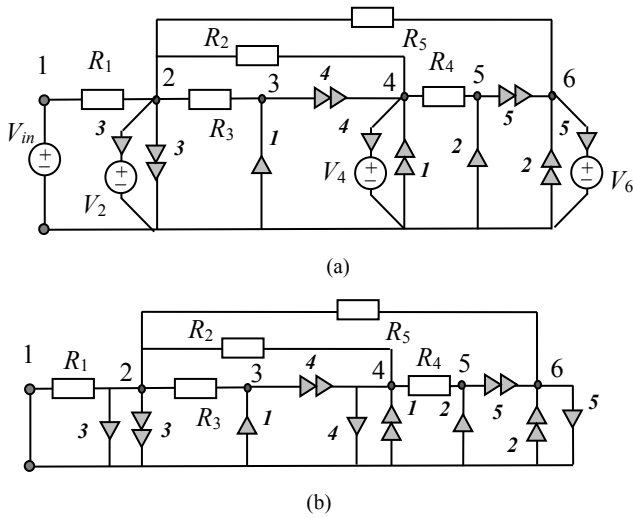


Fig. 5. (a) Compensated circuit; (b) Determinant of compensated circuit.

Now let's calculate the determinant of denominator circuit. The resistance R_4 is connected in series with nullator marked by 2 and can be shorted. The mutual interchanging of the norators marks 1 and 2 provide the shorting of nullor elements marked by number 2 and changing the sign of expression. Then parameter \underline{V}_4 can be extracted and voltage source can be replaced by norator marked by number 5. In that case the parameters of all other controlled sources are null. Now the parameters R_1, R_2, R_3 и R_5 are extracting and corresponding resistors are deleting. The determinant of residual circuit is equal to unity. So the symbolic expression of denominator will be as follow:

$$D = R_1 R_2 R_3 R_5 \underline{V}_6. \quad (19)$$

After substitution of expressions (18) and (19) to circuit-algebraic formula (17) and cancellation of equal terms the formula for unknown resistance can be expressed as:

$$R_6 = -R_4 \underline{V}_6 / \underline{V}_4. \quad (20)$$

Symbolic cancellation-free expressions for other unknown parameters have been calculated by means of Cirsym:

$$C_1 = -(-R_5 R_4 \underline{V}_1 R_2 R_3 + R_4 \underline{V}_2 (R_1 (R_2 (R_3 + R_5) + R_3 R_5) + R_2 R_3 R_5 + R_1 (-R_2 R_3 R_4 \underline{V}_6 - R_3 R_4 R_5 \underline{V}_4)) / (p R_1 R_5 R_2 R_4 R_3 \underline{V}_2);$$

$$C_2 = \underline{V}_2 / (-p R_3 \underline{V}_4). \quad (21)$$

We will calculate the symbolic expressions for voltages $\underline{V}_2, \underline{V}_4$ and \underline{V}_6 in nullor equivalent circuit in Fig. 5 (b) by means of Cirsym to verify the obtained results:

$$\underline{V}_2 = \underline{V}_1 R_2 R_5 R_4 R_3 p C_2 / (p C_2 (R_1 R_3 p C_1 + R_1 + R_3) R_2 R_5 R_4 + R_1 R_3 p C_2 (R_2 + R_5) R_4 - R_1 (R_2 R_6 - R_4 R_5));$$

$$\underline{V}_4 = -R_5 R_4 \underline{V}_1 R_2 / (p C_2 (R_1 R_3 p C_1 + R_1 + R_3) R_2 R_5 R_4 + R_1 R_3 p C_2 (R_2 + R_5) R_4 - R_1 (R_2 R_6 - R_4 R_5));$$

$$\underline{V}_6 = R_5 R_6 \underline{V}_1 R_2 / (p C_2 (R_1 R_3 p C_1 + R_1 + R_3) R_2 R_5 R_4 + R_1 R_3 p C_2 (R_2 + R_5) R_4 - R_1 (R_2 R_6 - R_4 R_5)). \quad (22)$$

After substitution of voltages expressions to formulae of unknown parameters one can obtain the identities $R_6 = R_6,$

$C_1 = C_1$ и $C_2 = C_2$. So the formulae (14) and (15) provide the numerical result of fault diagnosis

Unlike of numerical methods of diagnosis the accuracy of proposed symbolic technique depends only on precision of known parameters and measured currents and voltages.

V. CONCLUSIONS

The symbolic analysis technique based on Generalized Parameter Extraction Method successfully implemented in parametric fault diagnosis of analog electrical circuits. Algorithm for automatic fault diagnosis is presented. Symbolic solution obtained by proposed algorithm is cancellation-free and provides the simple test for solvability. Presented fault diagnosis algorithm has been implemented by V. Filartov in symbolic circuit analyzer Cirsym.

REFERENCES

- [1] J. A. Starzyk, Dong Liu, Zhi-Hong Liu, D. Nelson and J. Rutkowski, "Entropy-based optimum test points selection for analog fault dictionary techniques," IEEE Transactions on Instrumentation and Measurement, vol. 53, no. 3, pp. 754-761, June 2004.
- [2] A. Zhirabok and A. Baranov, "Fault Diagnosis in Analog Electrical Circuits: Data-Driven Method," in Proc. of International Conference on Process Control (PC), Štrbské Pleso, Slovakia, pp. 90-95, June 2013.
- [3] Z. Kolka, V. Biolkova, Z. Kincl, and D. Biolk, "Parametric reduction of Jacobian matrix for fault analysis," in Proc. of International Conference on: Microelectronics (ICM), Cairo, Egypt, pp. 503 - 506, Dec. 2010.
- [4] Z. Kincl and Z. Kolka, "Approximate Parametric Fault Diagnosis," in Proc. of 21st International Conference Radioelektronika (RADIOELEKTRONIKA), Brno, Czech, pp. 1 - 4, April 2011.
- [5] H. Hu, S. Tian, Q. Guo and A. Ouyang "The Application of HIWO-SVM in Analog Circuit Fault Diagnosis," International Journal of Pattern Recognition and Artificial Intelligence, vol. 29, no. 8, 27 p., 2015.
- [6] M.-H. Wang, "Application of Extension Neural Network Type-1 to Fault Diagnosis of Electronic Circuits," Mathematical Problems in Engineering, vol. 2012, Article ID 352749, pp. 1-12, 2012.
- [7] V. Prasannamoorthy and N. Devarajan, "Fault detection and classification in power electronic circuits using wavelet transform and neural network", Journal of Computer Science, vol. 7, pp. 95-100, 2011.
- [8] T. Ozawa and Y. Kajitani, "Diagnosability of linear active networks," IEEE Trans. Circuit and Syst., vol. 26, no 7, pp. 485 - 489, 1979.
- [9] S. L. Farchy, E. D. Gadzheva, L. H. Raykovska, and T. G. Kouyoumdjiev, "Nullator-norator approach to analogue circuit diagnosis using general-purpose analysis programmes," International Journal of Circuit Theory and Applications, vol. 23, is. 6, pp. 571-585, 1995.
- [10] F. Grasso, A. Luchetta, S. Manetti and M.C. Piccirilli, "A method for the automatic selection of test frequencies in analog fault diagnosis", IEEE Transactions on Instrumentation and Measurement, vol. 56, pp. 2322 - 2329, Dec. 2007.
- [11] J. A. Starzyk, Topological Analysis and Diagnosis of Analog Circuits, Wydawnictwo PŚ, 147 p., 2007.
- [12] S. Manetti, and M.C. Piccirilli, "Symbolic function approaches for analogue fault diagnosis," in Test and diagnosis of analogue, mixed-signal and RF integrated circuits, Yichuang Sun, Ed. London: IET-The Institution of Engineering and Technology, 2008, Ch. 2.
- [13] S.A. Kurganov, "A symbolic approach to solving the problem of linear electronic circuit diagnostics," Electrical technology Russia, vol. 3, pp. 70-77, 2002.
- [14] V. Filartov and A. Korotkov, "Generalized parameter extraction method in symbolic network analysis," in Proc. of ECCTD, Kraków, Poland, vol. 2, pp. 406-409, Sept. 2003.
- [15] V. Filartov and A. Korotkov, "Generalized parameter extraction method in case of multiple excitation," in Proc. of SMACD'04, Wrocław, Poland, pp.8-11, Sept. 2004.