The simulation technique for large-scale tree structured interconnects

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***Abstract*— An accurate and efficient method for modeling and analysis of on-chip interconnects is presented in this paper. The proposed technique is based on circuit decomposition approach and provides the recursive calculation of *T*-tree transfer function. The symbolic expressions of voltage transfer functions of the large-scale integrated interconnect structures are determined. To demonstrate the validity of the proposed method, lumped *T*-tree networks of different levels for the microelectronic interconnect application are simulated. Excellent agreement between the modeling results and SPICE-computations is found both in frequency- and time-domains.**

Keywords—circuit simulation, symbolic analysis, discrete line model, high-speed interconnections, very large scale integration (VLSI).

I. INTRODUCTION

The continuous miniaturization of integrated circuits make possible the massive systems-on-chip integration. The composition of the modern circuit becomes more and more sophisticated and the most complicated structure is the on-chip interconnect which links millions of logic gates. The performance of circuits such as propagation delay and power consumption is highly dependent on interconnects [1-4]. For signal transmission the non-ideal effects of interconnections like frequency dispersion loss and noise can be causes of distortions, errors and asynchronous effects [2].

So, for electronic circuit design it is necessary to analyze and model the time and frequency characteristics of the interconnects. Various techniques based on either simulation techniques or analytical formulas have been proposed for the analysis of interconnections. Simulation tools such as SPICE give the accurate insight into arbitrary interconnect structures but are computationally expensive.

An interconnection system can be described by means of its electrical parameters. Over the years, extensive work has been done in developing models that combine computational accuracy and simplicity [2-13]. The equivalent circuit model can take a variety of forms: resistance–capacitance (*RC*) or resistance–inductance–capacitance (*RLC*) tree with grounded capacitances, capacitively and/or inductively coupled *RLC* trees or mesh networks involving resistive links and driven by multiple independent sources. These interconnection structures cover almost all of interconnect systems in practice. Most popular of them is well-known Elmore *RC* model [5] of *T*-tree shown in Fig. 1 in general form. But for a high frequency applications inductive effects become significant and for sufficient description of the interconnects the *RLC* model must be used [2].

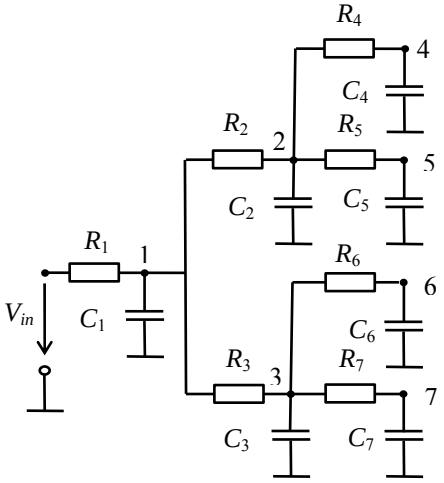

Fig. 1. A general *RC*-tree.

Most of the interconnections analysis techniques have deals with approximation of transient response at the nodes of *RLC*-tree [6-9]. One of the simplest existing delay models for *RLC*-tree has been proposed by Ismail and Friedman [6]. But this two-pole model provides calculation of far end time domain response only for single-line interconnect. In [7], the method of low-frequency approximation of the transfer function for a tree structured interconnects is presented. The method is based on directly truncating the higher powers of *s* in the numerator and denominator of the network function. But some of the poles determined using the direct truncations can be unstable and need to be discarded from the computation.

The methods based on moment matching approach have been widely used in solving complex interconnect structures [10]. Moment matching provides the reduced-order modeling of massive interconnect systems. With transmission line effects becoming more significant, additional *RLC* segments need to be used to behavior simulation of the distributed interconnect. The computational efficiency of these methods

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will be decreased, making them uneasy to use for interconnect analysis in early design stages.

Another approach to analysis of interconnection system proposed in [11-13]. The method provided the accurate analytical calculation but required the transformation of single input multiple output (SIMO) *RLC* model to reduced single input single output (SISO) circuit equivalent. Transformation of circuit leads to parameters transformation that can increase the inaccuracy and complexity of numerical calculation.

In this paper the direct symbolic technique for analysis of large-scale *RC* and *RLC* interconnection trees is proposed. The analysis concept presented in Section II is based on circuit decomposition approach [14] and Generalized Parameter Extraction Method (GPEM) [14-19]. In Section III, the proposed technique is applied to simulation of interconnect trees of different levels, and the results are compared with SPICE.

II. Description of Method

A. Topological analisys of L-cells

The general *RC*-tree shown in Fig. 1 is a typical SIMO circuit consisted of lumped *L*-cells formed by *R*-series resistance and *C*-parallel capacitance. In Fig. 2 (a) and Fig. 2 (b) the *L*-cells with arbitrary admittances g and y are presented as short and open circuits correspondingly. The network determinants D_1 and ${}^{op}D_1$ are also given. One can say that the *L*-cell is the first-level *RC*-tree.

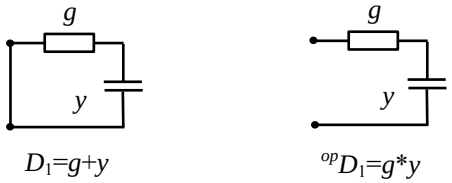


Fig. 2. *L*-cells with shorted and opened input.

Let's consider the SISO ladder circuit composed of k-number *L*-cells shown in Fig. 3. In accordance with GPEM [14-19] the network function of any linear circuit can be expressed as following:

$$H(p)=\frac{N(p)}{D(p)}, \qquad (1)$$

where $N(p)$ is the determinant of the circuit, in which the input voltage V_{in} and output response V_{out} are replaced by nullor, and $D(p)$ is the determinant of the circuit, in which the V_{in} and V_{out} are turned to zero.

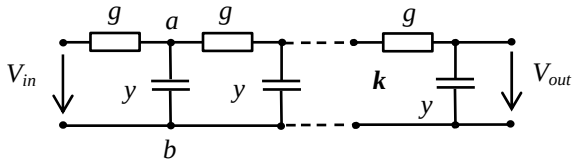


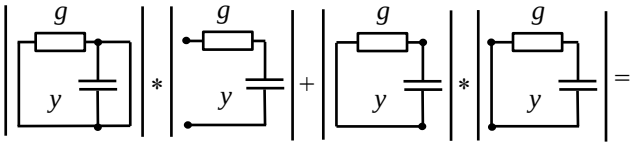
Fig. 3. Ladder circuit.

The circuit structure can be divided into two subcircuits by means of the decomposition formula [14]:

$$\Delta = \Delta_1(a,b)\Delta_2 + \Delta_1\Delta_2(a,b), \qquad (2)$$

where $\Delta_1(a,b)$ and $\Delta_2(a,b)$ are determinants of first and second subcircuits in which the nodes a and b are shorted, Δ_1 and Δ_2 are determinants of subcircuits in which the nodes a and b are opened.

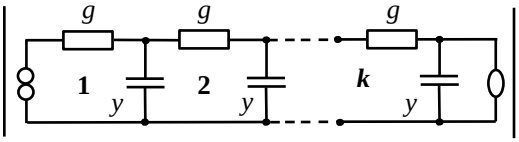
The determinant D_{L2} of the second level ladder circuit can be calculated by means of formula (2) as following:

$D_{L2}=$  $=$

$$= 1 * {}^{op}D_1 + D_1 * D_1 = {}^{op}D_1 + (D_1)^2 = g*y+(g+y)^2. \qquad (3)$$

One can see that in case of ladder circuit decomposition by nodes a and b the expression (3) is consists of circuit determinants of short and open *L*-cells. If the decomposition of k-level ladder circuit is always performed by nodes a and b shown in Fig. 3 than determinants of expressions (2) can be expressed as follow: $\Delta_1(a,b) = 1$, $\Delta_2 = {}^{op}D_{L(k-1)}$, $\Delta_1=D_1$, $\Delta_2(a,b) = D_{L(k-1)}$.

Determinant expansion of numerator N_L of ladder circuit transfer function is pretty simple. Parameters of admittance elements connected in series with norator or nullator are expanding as multiplier coefficient, admittances parallel to one of the nullor elements are deleting [14-19]. So the numerator of transfer function of k-order ladder circuit can be calculated as following:

$N_{Lk}=$  $= g^k.$ (4)

B. Topological analisys of T-tree

Now let's consider the application of decomposition based analysis approach for a second-level symmetrical *T*-tree. The subcircuits for calculation of transfer function numerator and denominator are presented in Fig. 4 (a) and Fig. 4 (b) correspondingly.

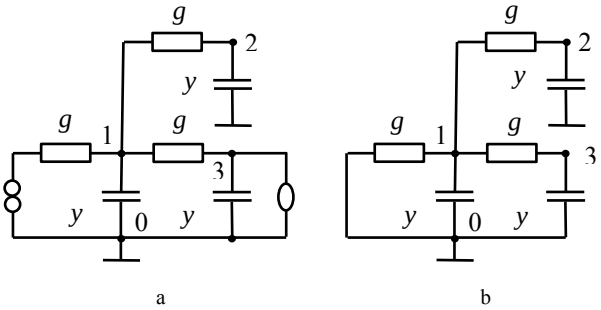
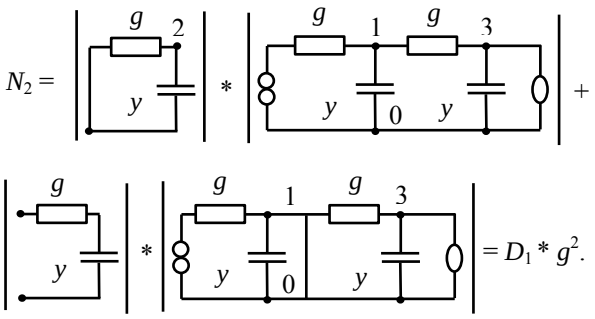
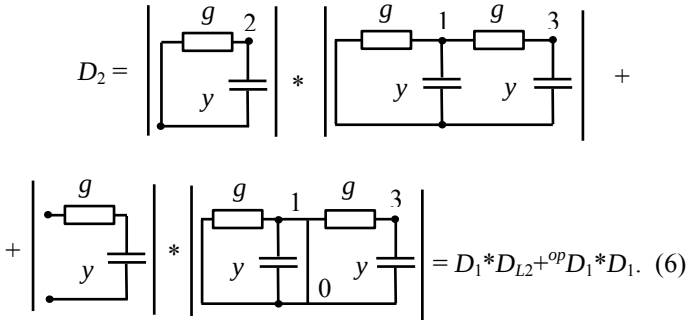


Fig. 4. Circuit equivalent for numerator (a) and denominator (b) of voltage transfer function of 2-level *T*-tree.

Decomposition of circuit depicted in Fig. 4 (a) by nodes «1» and «0» in accordance with formula (2) is shown below:



The symbolic expression of denominator D_2 is expanded in the same way:



The transfer function of second level *T*-tree can be expressed as:

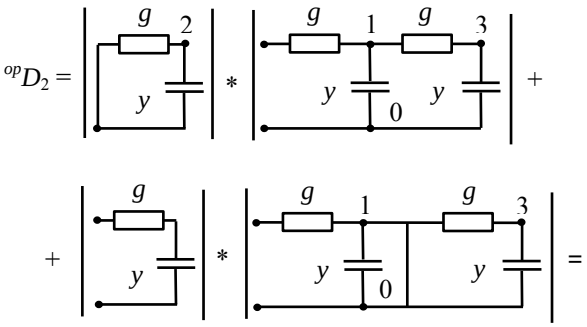
$$H_2 = \frac{N_2}{D_2} = \frac{g^2 D_1}{D_1(D_{L2} + {}^{op}D_1)} = \frac{g^2}{2\,{}^{op}D_1 + D_1^2} = \frac{g^2}{g^2 + 4gy + y^2}. \quad (7)$$

Let's suggest that decomposition of circuits and subcircuits by means of the formula (2) is always performed by nodes «1» and «0». Than in the general case the transfer function of *n*-level *T*-tree can be calculated by means of recurrent formula presented below:

$$H_n = \frac{N_n}{D_n} = \frac{g^n N_{(n-1)}}{D_{(n-1)}(2\,{}^{op}D_{(n-1)} + D_1 D_{(n-1)})}, \quad (8)$$

where D_1 is a determinant of *L*-cell presented in Fig. 1 (a), $N_{(n-1)}$ is a numerator of transfer function of *T*-tree of previous level, ${}^{op}D_{(n-1)}$ and $D_{(n-1)}$ are determinants of the short and open *T*-trees of *n*-1 level correspondingly.

Since the $D_{(n-1)}$ is just a denominator of transfer function $H_{(n-1)}$, the further explanation of calculation process of expression ${}^{op}D_{(n-1)}$ is needed. For example the expansion of determinant ${}^{op}D_2$ of the second-level open *T*-tree will be as follow:



$= D_1*(g* {}^{op}D_1 + {}^{op}D_1*D_1) + {}^{op}D_1*g*D_1 = D_1*(2g* {}^{op}D_1 + {}^{op}D_1*D_1).$ (9)

For the general case the determinant of open *T*-tree of *n*-level can be expressed as follow:

$${}^{op}D_n = D_{(n-1)}(2g\,{}^{op}D_{(n-1)} + {}^{op}D_1 D_{(n-1)}). \quad (10)$$

The numerator expression of transfer function of *n*-level *T*-tree will consists of the consequence of *n*-1 number of determinants:

$$N_n = g^n \cdot D_{(n-1)} \cdot D_{(n-2)} \cdot \ldots \cdot D_1. \quad (11)$$

One can see from (8) and (10) that determinants ${}^{op}D_n$ and D_n are including the expression $D_{(n-1)}$ as common multiplier. It is safe to say that each determinants ${}^{op}D_{(n-m)}$ and $D_{(n-m)}$, where $n>m$, will include the denominator of $H_{(n-m-1)}$ transfer function. So the expressions of N_n, ${}^{op}D_n$ and D_n can be simplified:

$$N'_n = g^n, \quad (12)$$

$$D'_n = 2\,{}^{op}D'_{(n-1)} + D_1 D'_{(n-1)}, \quad (13)$$

$${}^{op}D'_n = 2g\,{}^{op}D'_{(n-1)} + {}^{op}D_1 D'_{(n-1)}. \quad (14)$$

The transfer function of *n*-level *T*-tree will be expressed as follow:

$$H_n = \frac{g^n}{2\,{}^{op}D'_{(n-1)} + D_1 D'_{(n-1)}}. \quad (15)$$

The expression (15) can be recursively used for transfer function calculation of *T*-trees of any levels. There are only two determinants are needed for each iteration. In case of interconnection tree with number of levels more than three the following transformation of expression (15) will be appropriate:

$$H_n = \frac{g^n}{2(2g\,{}^{op}D'_{(n-2)} + {}^{op}D_1 D'_{(n-2)}) + D_1(2\,{}^{op}D'_{(n-2)} + D_1 D'_{(n-2)})} = \frac{g^n}{D'_{(n-2)}(2\,{}^{op}D_1 + D_1^2) + {}^{op}D'_{(n-2)}(4g + 2D_1)} = \frac{g^n}{D'_{(n-2)}D_2 + {}^{op}D'_{(n-2)}(4g + 2D_1)}. \quad (16)$$

The analytical transfer functions calculated by means of formula (16) are presented in Table I for various levels (n={3…10}) of T-tree network. The expressions for high level T-trees (n={3…100}) can be downloaded directly from the internet site intersyn.net/ttree.txt.

III. Examples

The simulation results of modeling distributed RC- and RLC-interconnection circuits are presented in this section. The results obtained by using Maple 18 are compared with LtSpice IV simulation. By reason of symmetry, the voltages, detected at the output terminals of the considered tree network are the same. The time domain step response estimation performed by Laplace transformation.

A. RC-trees simulation results

As a use case example, the RC long interchip interconnect with per unit length parameters R = 100 Ω, C = 0.35 pF [11-13] are taken in this section. The calculation performed for T-trees of five and ten levels. The parameters values in corresponding transfer functions from Table I are following: $g = 1/R$, $y = pC$.

As depicted in Fig. 5 and Fig. 6, an excellent agreement of the time-domain and frequency results was realized between the formulae from Table I computed in Maple programming environment and LtSpice IV simulations.

B. RLC-trees simulation results

With increasing on-chip signal frequencies, the effect of interconnect inductance has become more significant, particularly in global interconnects. Simulation of n-level RLC-trees performed for circuit parameters: R = 40 Ω, C = 0.1 pF, L = 7 nH [11-13]. The parameters values in corresponding transfer functions from Table I are following: $g = 1/(R+pL)$, $y = pC$.

Again the proposed models results are in good agreement with Spice simulations as it seems from Fig. 7 and Fig. 8.

IV. Conclusions

The symbolic technique for the symmetrical RLC-tree distribution networks analysis have been presented. Described method is based on the direct analytical calculation by means of the proposed recurrent formulae. Exact symbolic expressions of the T-tree network transfer functions were presented for the tree levels up to 10. Expressions of higher levels up to 100 can be downloaded from intersyn.net/ttree.txt. The calculation results of modeling examples are in good agreement with simulations by means of LtSpice IV. The proposed techique is simple and provide high computational accuracy and perfomance. It can be used for the signal integrity prediction during the design process of the microelectronic circuits.

TABLE I. Transfer functions of RC-tree for n={3…10}.

n	**Transfer function, $H_n(s)$**
3	$\frac{g^3}{g^3+11g^2y+7gy^2+y^3}$
4	$\frac{g^4}{g^4+26g^3y+30g^2y^2+10gy^3+y^4}$
5	$\frac{g^5}{g^5+57g^4y+102g^3y^2+58g^2y^3+13gy^4+y^5}$
6	$\frac{g^6}{g^6+120g^5y+303g^4y^2+256g^3y^3+95g^2y^4+16gy^5+y^6}$
7	$\frac{g^7}{g^7+247g^6y+825g^5y^2+955g^4y^3+515g^3y^4+141g^2y^5+19gy^6+y^7}$
8	$\frac{g^8}{g^8+502g^7y+2116g^6y^2+3178g^5y^3+2310g^4y^4+906g^3y^5+196g^2y^6+22gy^7+y^8}$
9	$\frac{g^9}{g^9+1013g^8y+5200g^7y^2+9740g^6y^3+9078g^5y^4+4746g^4y^5+1456g^3y^6+260g^2y^7+25gy^8+y^9}$
10	$\frac{g^{10}}{g^{10}+2036g^9y+12381g^8y^2+28064g^7y^3+32354g^6y^4+21504g^5y^5+8722g^4y^6+2192g^3y^7+333g^2y^8+28gy^9+y^{10}}$

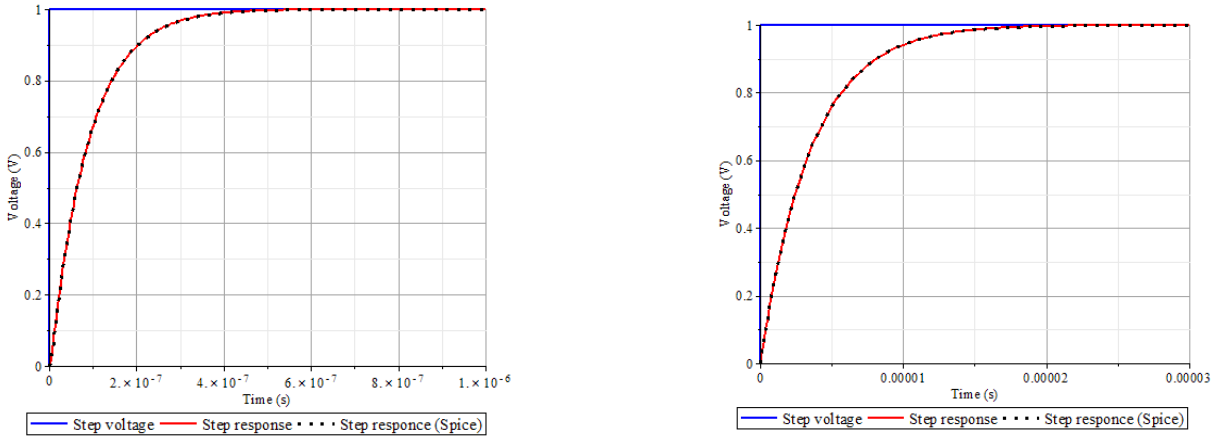


Fig. 5. Time domain response of *RC*-tree interconnect: (a) 5-level tree, (b) 10-level tree.

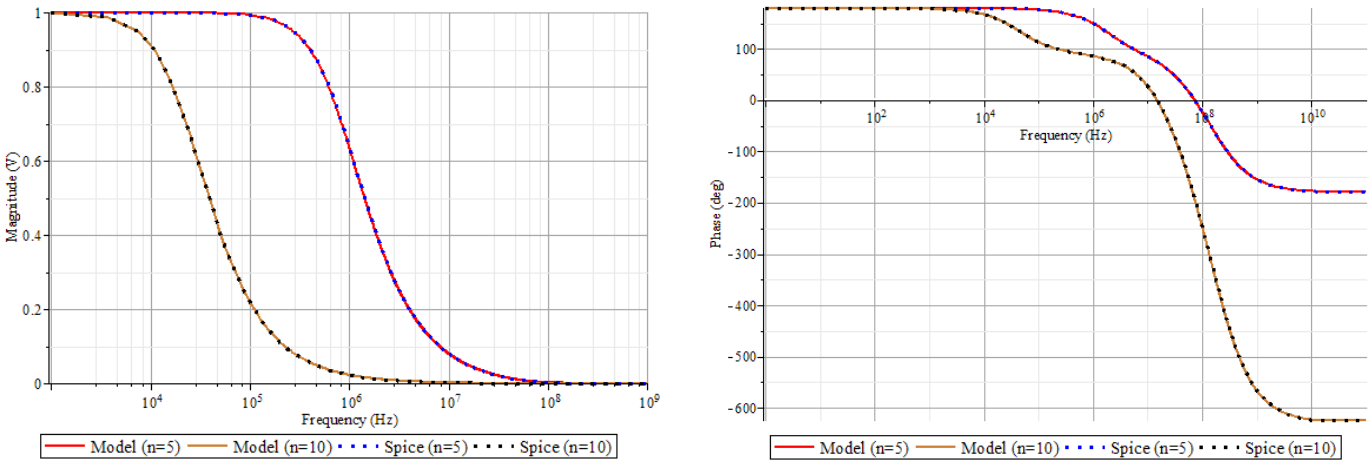


Fig. 6. Comparisons of LtSpice IV and the proposed model frequency results of identical lumped *RC*-tree network for $n = 5$ and $n = 10$. (a) Magnitude- and (b) phase-responses.

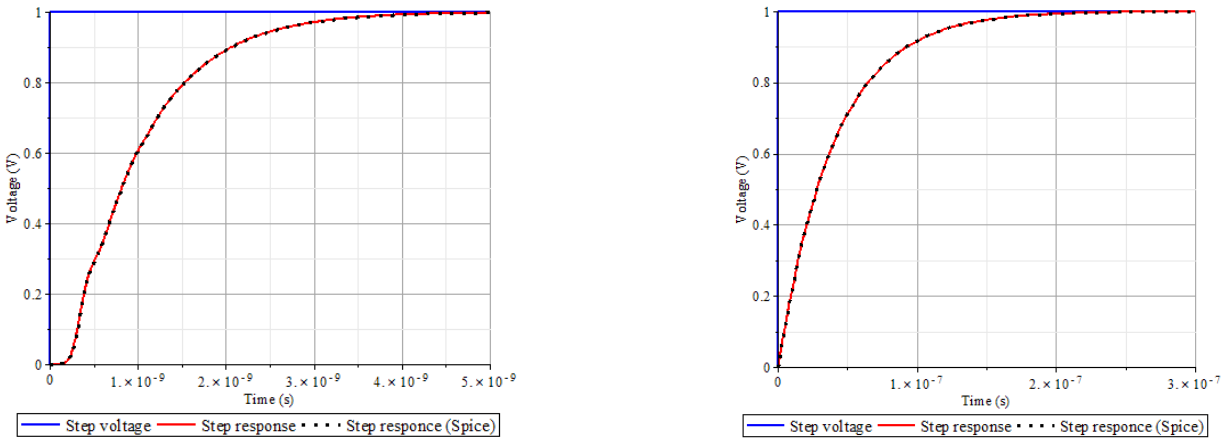
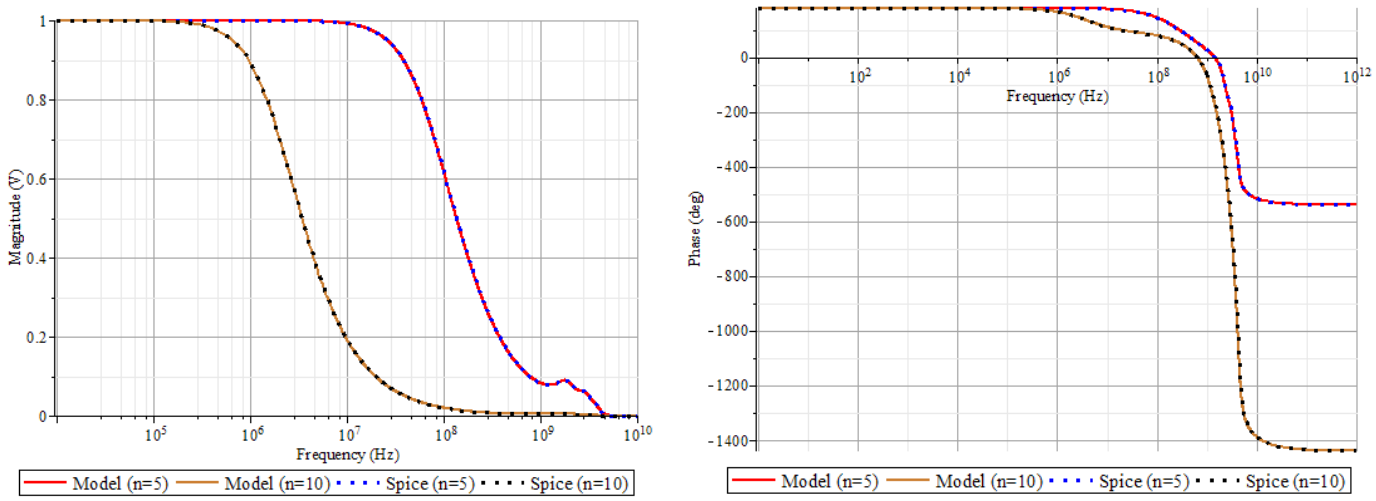


Fig. 7. Time domain response of *RLC*-tree interconnect. (a) 5-level tree, (b) 10-level tree.



a b

Fig. 8. Comparisons of LtSpice IV and the proposed model frequency results of identical lumped *RLC*-tree network for $n = 5$ and $n = 10$. (a) Magnitude- and (b) phase-responses.

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