A circuit synthesis technique based on network determinant expansion

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Abstract — **In this paper we present a simple technique of analog electronic circuits synthesis by means of a linear representation. The approach is based on generalized parameter extraction method. It describes the procedure for developing the circuit topology both for passive or active circuits. The input data for the proposed synthesis method are the arbitrary network function approximated in polynomial form and specified elements set. In contrast to other synthesis approaches the proposed technique provides the realization of full set of equivalent circuits and allow to choose the best circuit solutions by various criteria. Experiments conducted on the low-pass filter design demonstrate the simplicity and effectiveness of synthesis method.**

Keywords - circuit synthesis, network function, symbolic circuit analysis, network determinant.

I. INTRODUCTION

Analog circuits are of great importance in electronic system design since every process in material world has an analog nature. Most of electronic circuits deploy analog networks as essential building blocks. But unlike digital design, analog design mainly rests on the expertise of specially trained experts. The design process is an exhaustive, knowledge-intensive and iterative task that takes considerable time even by experienced designers. That is why analog-based CAD tools develop very slowly as compared to the digital ones [1].

Circuit synthesis is defined as the process of constructing circuits that satisfies the desired performance specifications. The goal of analog circuit synthesis tools is to eliminate most tedious tasks. The main problem of automation synthesis technique is to evolve the circuit topologies and obtain the best one. It is obvious that the circuit design is an ambiguous task. So it is desirable that the circuit synthesis techniques can evolve and maintain the full set of possible circuit solutions.

Techniques for analog circuit design automation appeared about four decades ago. These methods incorporated heuristics [2], knowledge-bases [3, 4], simulated annealing [5], and evolutionary computation [6, 7]. Unfortunately all of them have some limits for circuit topologies and cannot provide the full set of possible circuit solutions in general case.

In this paper we propose a new method of evolving analog electronic circuits by means of a linear representation providing the realization of the full equivalent circuits set corresponding to the given polynomial network function. The approach is based on symbolic circuit analysis technique named «generalized parameter extraction method» [8, 9]. Section II describes the proposed circuit synthesis technique. Section III demonstrates the effectiveness of the synthesis method by means of low-pass filter design example. The conclusion is finally drawn in Section IV.

II. DESCRIPTION OF THE SYNTHESIS TECHNIQUE

The proposed circuit synthesis approach is shown in Fig. 1. The input data for the synthesis technique are the specified elements set and rational expressions N(p) and D(p) of the arbitrary network function approximated in polynomial form

$$S(p)=\frac{N(p)}{D(p)}=\frac{a_n p^n+a_{n-1}p^{n-1}+\ldots+a_0}{b_n p^n+b_{n-1}p^{n-1}+\ldots+b_0}, \qquad (1)$$

where N (p) is the determinant of the circuit, in which the independent source and arbitrary response are replaced by nullor, and D(p) is the determinant of the circuit, in which the independent excitation and the arbitrary response are zero [10].

Also we can use the synthesis specifications: the elements number of each type that should be used in synthesis process or some of the optimal number criteria of elements: a) $C\rightarrow$min; b) $L\rightarrow$min; c) $R\rightarrow$min; d) controlled sources (CS)$\rightarrow$min.

The individual aspects of synthesis stages are detailed in the following subsections.

A. Expansion of network function denominator

The network function denominator can be expanded until the determinant of the simplest circuit (Fig. 2) will be derived

$$D_n=b_n p^n+D_{n-1},\quad D_{n-1}=b_{n-1}p^{n-1}+D_{n-2},\ \ldots,$$
$$D_1=b_1 p+D_0,\quad D_0=b_0, \qquad (2)$$

where D_0, D_1,…, D_{k-1} are subcircuits determinants of designed circuits that corresponds with expression D_n. The expression number in expansion (2) is equal to amounts of reactive elements in the corresponding subcircuit.

So the result of expansion (2) will be the expression D1 or D0. The circuit the determinant of which corresponds with this expression we name as the initial circuit. It is obvious that D1 is the determinant of the circuit consisting only of one reactive element and D0 is the determinant of the circuit consisting of nonreactive elements.

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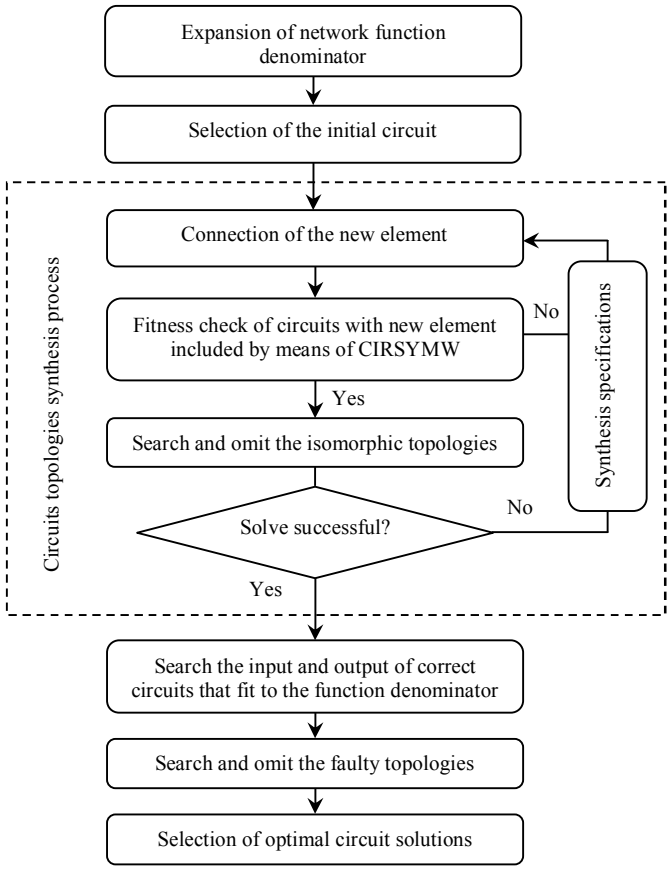


Fig. 1. Synthesis approach

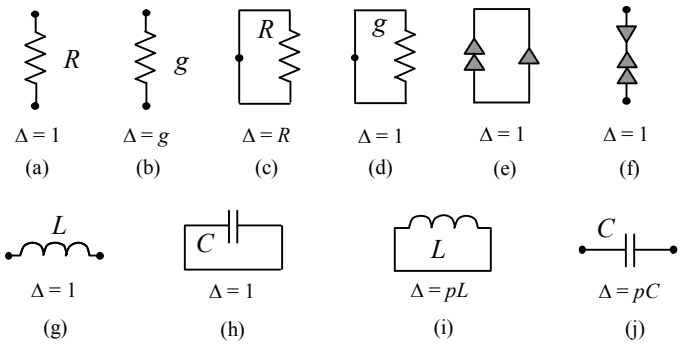


Fig. 2. The initial circuits and their determinants

B. *Selection of the initial circuit*

If the types of the elements in the desired circuits are specified, then the initial circuit can be chosen in accordance with the following rules: 1) if coefficients $b_0 \neq 0$, $b_1 \neq 0$, the initial circuits chosen from Fig. 2 are (a)–(f); 2) if coefficients $b_0 \neq 0$, $b_1=0$, the initial circuits chosen from Fig. 2 are (g) or (h); 3) if coefficients $b_0 = 0$, $b_1 \neq 0$, the initial circuits chosen from Fig. 2 are (i) or (j).

C. *Circuits topologies synthesis process*

1) Connection of the new element. When the initial circuit is defined we can try to connect any of two-ports or controlled sources from specified elements set to this topology. There are four ways of elements connection: in series, in parallel, as short-circuit or as an open loop. The CS will be connected as a system of two-ports: the source and the controlled signal are injected in the circuit together.

2) Fitness check by means of generalized parameter extraction method. The determinants of obtained circuits with new element included may corresponds to the expressions of expansion (2) numbers of which are equal to reactive elements amounts. This kind of circuits we name as correct circuits. For example, for the expression $D_2 = b_2p^2 + b_1p - b_0$ the polynomial coefficients of correct circuits determinants must be $b_0 < 0$, $b_1 > 0$, $b_2 > 0$. The process of selection of corrected circuits by means of comparison of symbolic determinant coefficients with the coefficients of expressions from expansion (2) we consider as fitness check.

The most convenient analysis approach for the fitness process is a generalized parameter extraction method, because it provide the obtaining of symbolic circuit determinants in rational polynomial form.

The calculation procedure of the circuit determinants is based on the recursive usage of the parameter extraction formula which generalizes the Feussner's equations [11, 12]:

$$\Delta = \chi\Delta(\chi \to \infty) + \Delta(\chi = 0) \qquad (3)$$

where χ is a parameter of arbitrary circuit element, $\Delta(\chi\to\infty)$ and $\Delta(\chi = 0)$ corresponds to the determinants of the circuit matrix in which the parameter of extracted elements $\chi\to\infty$ or $\chi = 0$ respectively.

In case when $\chi\to\infty$ the selected element must be omitted from the circuit if χ is an impedance, and replaced by a short or by a nullor if χ is a conductance or a controlled source correspondingly. In case when $\chi = 0$ the selected element must be replaced by a short if χ is an impedance, and deleted if χ is a conductance. If the selected element is a CS then in case when $\chi = 0$ voltage source and controlling current must be replaced by a short, but current source and controlling voltage must be deleted.

After the removal all passive and active elements from circuit by means of formula (3) the residual circuit will consist of one of two-ports as shown in Fig. 2, (a)–(d) and Fig. 2, (g)-(j) or a number of oriented nullors (Fig. 2, (e)–(f)) [13, 14]. The determinant of nullors circuit can be equal to 0 or ±1. It can be used to determine the sign of the determinants. The choice of the sign depends on the orientation of the nullator and norator. If these elements have got the same orientation the sign will be positive. In the opposite case the sign will be negative [8, 9].

The generalized parameter extraction method is an effective tool for circuit symbolic analysis [8, 9, 15] and synthesis [16, 17]. The method has been realized in the symbolic circuit analysis program CIRSYM (http://intersyn.narod.ru/scad.htm) that used for the automatization of the fitness check process.

Suppose that we include some element to the initial circuit that correspond to expression D0, and obtain the correct circuits that fits to D1. Then we can connect the element of

another type to each of the obtained correct circuits and find the set of topologies that may include the correct circuits corresponding to D2. The faulty circuits must be omitted. In case when the including of the element of one type does not provide the obtaining of any correct circuit at all we should try again with another element type. We recommend the including of two-ports in first order. It is desirable that two-ports of different types should be connected one by one. Then obtained circuit solutions will be optimal by reactive elements amount in the consequence of expansion (2). Of course, it is possible to add more reactive elements in circuit as capacitors loops or inductances sections if necessary.

3) Search and omit the isomorphic topologies. If we continue the elements connection checking new circuits step by step we`ll finally find the full set of correct circuits that fit with the denominator of (1) [17]. Of course if that kind of circuits will ever exist. But some of these circuits may be isomorphic. So it is necessary to find and omit such circuits every time after a new element is included [17]. The obtaining of the set of non-isomorphic circuits equivalent by network determinant and by the elements amount will be the successful solution of the circuit topologies synthesis process.

D. Search the input and output of correct circuits

If we search the input and output of every circuit that fit to the expression D_n in accordance with the type of the network function (1) then the correct circuits from the obtained set will be the equivalent by network function. This procedure can be done by means of connecting some voltage (current) source as input and an ideal voltmeter (ammeter) as output to the circuit.

E. Search and omit the faulty topologies

The faulty topologies must be defined in accordance with the following criteria: a) the topologies can be bisected by deleting of one node; b) the topologies include the short-circuits or open loops; c) the topologies include faulty connected CS (the parameter of CS will be omitted from the symbolic network function, so the circuit can be corrected formally, but will not work properly); d) the topologies include the CS that is not connected to the ground node.

F. Selection of optimal circuit solutions

The optimal circuit solutions must be defined by following procedures: 1) parameters synthesis by solving the system of nonlinear equations; 2) gain-frequency and phase(-response) characteristics analysis; 3) symbolic tolerances analysis [15].

The proposed method has been realized in the circuit synthesis program InterSyn (http://intersyn.narod.ru) as a part of the software tool SCADS. The experiments with program have shown that the full set of non-isomorphic circuits equivalent by polynomial network function may include some circuits equivalent by symbolic network function as well. We have determined that this is possible only when the elements set involve CS of dual types (the voltage source will be dual for current source, and the controlled voltage will be dual for controlled current). On other hand there is no way to obtain the non-isomorphic circuits with the same symbolic network function if the elements set consist only of the resistance and reactance elements.

III. Synthesis Example

In this section we present the example of high-pass filter synthesis as an illustration of simplicity and effectiveness of proposed method. Suppose that our task is to evolve the circuit with certain gain-frequency characteristic and phase characteristic that can be approximated by means of polynomial function:

$$S(p) = p^3 /(p^3 + 10^3 p^2 + 5\cdot 10^5 p + 10^8). \quad (4)$$

Let's transform the function as follows and make the denominator expansion:

$$S(p) = 10^{-8} p^3 /(10^{-8} p^3 + 10^{-5} p^2 + 0.005p + 1). \quad (5)$$

$$D_0 = b_0, D_1 = b_1 p + D_0, D_2 = b_2 p^2 + D_1, D_3 = b_3 p^3 + D_2. \quad (6)$$

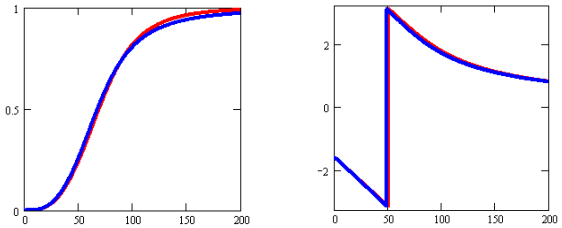
Suggest that the specified elements set consist of resistors, capacitors and two operational amplifiers. So, by means of the rules 1–3 we can choose the one of topologies from Fig. 2, (a) or (c) as the initial circuit. Then in accordance with block-scheme in Fig. 1 the circuit synthesis process deals with including of new elements from specified set and with fitness check of obtained circuits as it shown in Table I. After the search of input and output we obtained the optimal topologies of the third-order Bessel high-pass filter.

Elements values can be estimated by means of solution of the component equations system:

$$R_1R_2R_3C_1C_2C_3=10^{-8}, C_2(C_1R_1R_3+R_3C_3R_2)+C_3R_3C_1R_1=10^{-5},$$

$$C_2R_3+C_3R_3+C_1R_1 = 0.005.$$

The values obtained by means of InterSyn: R_1=2.4kΩ, R_2=3.4kΩ, R_3=1.3kΩ, C_1=C_2=C_3=100nF. The gain-frequency and phase(-response) characteristics of the given polynomial function (4) (red line) and the obtained network function (blue line) are shown in Fig 3.



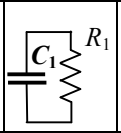
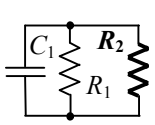
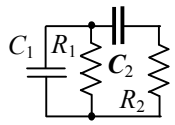
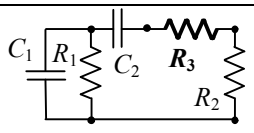
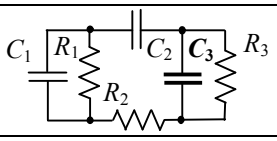
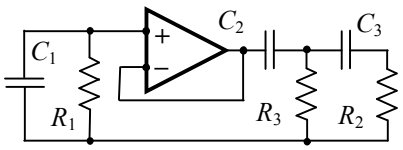
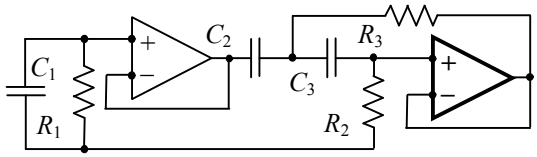
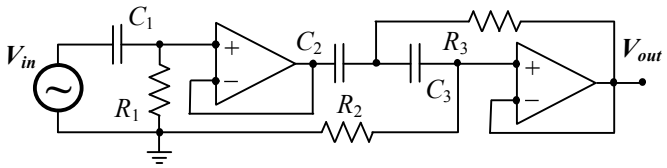
(a) (b)

Fig. 3. The gain-frequency (a) and phase(-response) (b) characteristics

V. Conclusions

We have presented a technique of circuit synthesis based on generalized parameter extraction method. Unlike the other synthesis approaches the proposed method provides realization of full set of electronic circuits equivalent by polynomial network function. There is no any limitation by linear elements type or by network function type. The selection criterion of the best circuit solutions has been offered. The proposed method can be useful for analog circuit design of electronic devices of different kind (filters, oscillators, amplifiers, and many others).

TABLE I. EXAMPLE OF THE HIGH-PASS FILTER SYNTHESIS

Stage	**1**	**2**	**3**	**4**	**5**
Included element	C_1	R_2	C_2	R_3	C_3
Corrected circuits					
Network determinant	$D_1=$ pC_1R_1 $+1$	$D_1=pC_1R_1R_2+$ R_1+R_2	$D_2= p^2\ C_2C_1R_1R_2$ $+p(C_2(R_1+R_2)+$ $C_1R_1)+1$	$D_2= p^2\ C_2C_1R_1(R_2+$ $R_3)+p(C_2(R_1+R_2+$ $R_3)+C_1R_1)+1$	$D_3= p^3\ C_1R_1C_2C_3R_2R_3+ p^2\ (C_1(R_1(C_2(R2$ $+R3)+C_3R_3))+C_2(C_3((R_1+R_2)R_3)))+$ $p(C_1R_1+C_2(R_1+R_2+R_3)+C_3R_3)+1$
Stage	**6**			**7**	
Included element	$OpAmp_1$			$OpAmp_2$	
Corrected circuits					
Network determinant	$D_3= p^3\ C_2R_3C_3R2C_1R_1+ p^2\ (C_2(R_3C_3R_2+C_1R_1)+$ $C_3(R_2+R_3)C_1R_1)+p(C_2R_3+C_3(R_2+R_3)+C_1R_1)+1$			$D_3= p^3\ C_2C_1R_1R_3C_3R_2+ p^2\ (C_2(C_1R_1R_3+$ $R_3C_3R_2)+C_3R_3C_1R_1)+p(C_2R_3+C_3R_3+C_1R_1)+1$	
Stage	**8**				
Included element	V_{in} **and** V_{out}				
Third-order Bessel high-pass filter					
Network function	$p^3\ R_2C_1R_1C_3R_3C_2 / p^3\ R_2C_1R_1C_3R_3C_2+ p^2\ (C_2(C_1R_1R_3+R_3C_3R_2)+C_3R_3C_1R_1)+p(C_2R_3+C_3R_3+C_1R_1)+1$				

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